

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

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Listing of Claims:

1 Claim 1 (currently amended). A method for designing at least one
2 mask for manufacturing an integrated circuit comprising:
3 generating a schematic for the integrated circuit, the integrated
4 circuit comprising a set of transistors;
5 entering data representing each transistor of the set into a
6 computer-aided design system;
7 identifying a first subset of the set of transistors implementing an
8 analog circuit comprising a cascode wherein the transistors of the first
9 subset are expected to be subject to voltage levels beyond the bounds of
10 a power rail and a ground rail of the integrated circuit during normal
11 operation;
12 designating, in the computer-aided design system, robust
13 geometries for the transistors of the first subset;
14 and
15 operating the computer-aided design system to generate the at
16 least one mask.

1 Claim 2 (original). The method of claim 1 further comprising:
2 identifying a second subset of the set of transistors, wherein the
3 transistors of the second subset are input-output transistors

4 and
5 designating, in the computer aided design system, robust
6 geometries for the transistors of the second subset.

1 Claim 3 (currently amended). An integrated circuit comprising:
2 a semiconductor die formed using at least one mask designed by
3 the acts of:
4 generating a schematic for the integrated circuit, the integrated
5 circuit comprising a set of transistors;
6 entering data representing each transistor of the set into a
7 computer-aided design system;
8 identifying a first subset of the set of transistors implementing an
9 analog circuit comprising a cascode wherein the transistors of the first
10 subset are expected to be subject to voltage levels beyond the bounds of
11 a power rail and a ground rail of the integrated circuit during normal
12 operation;
13 designating, in the computer-aided design system, robust
14 geometries for the transistors of the first subset, such that the set of data
15 may be used to generate a plurality of masks for lithography of features
16 having mutually different minimum line widths.

1 Claim 4 (currently amended). The integrated circuit of claim 3 wherein:
2 the at least one mask is designed by acts further comprising:
3 identifying a second subset of the set of transistors, wherein the
4 transistors of the second subset are input-output transistors
5 and

6 designating, in the computer aided design system, robust
7 geometries for the transistors of the second subset.

1 Claim 5 (currently amended). The integrated circuit of claim 3 wherein:
2 the integrated circuit implements a radio frequency circuit.

1 Claim 6 (currently amended). The integrated circuit of claim 4 3
2 wherein:
3 the integrated circuit implements a hybrid circuit.

1 Claim 7 (currently amended). The integrated circuit of claim 3 wherein:
2 the semiconductor die comprises metal-oxide transistors is formed
3 using lithography.

1 Claim 8 (currently amended). A method for designing a plurality of
2 masks for manufacturing an integrated circuit migrated across a plurality of
3 feature size technologies, each mask associated with a respective feature size
4 technology, the method comprising:
5 generating a schematic for the integrated circuit, the integrated
6 circuit comprising a set of transistors;
7 entering data representing each transistor of the set into a
8 computer-aided design system;
9 identifying a first subset of the set of transistors implementing an
10 analog circuit comprising a cascode wherein the transistors of the first
11 subset are expected to be subject to voltage levels beyond the bounds of

12 a power rail and a ground rail of the integrated circuit during normal
13 operation;
14 designating, in the computer-aided design system, robust
15 geometries for the transistors of the first subset;
16 and
17 operating the computer aided design system to generate a first
18 mask associated with a first feature size technology and a second mask
19 associated with a second feature size technology, wherein a respective
20 geometry of each transistor of the first subset is the same for both the first
21 mask and the second mask.